Amendments to the Claims

Please add new Claims 54-56. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (previously presented) A router including buffers, for information units transferred through the router, comprising:

a first set of rapidly accessible buffers which store information units received at an input link; and

a second set of buffers for the information units that are accessed more slowly than the first set;

the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.

2. (previously presented) A router as claimed in claim 1 wherein:

router processing is implemented on one or more router integrated circuit chips;

the first set of buffers is located on the router integrated circuit chips; and

the second set of buffers is located on memory chips separate from the router integrated circuit chips.

3. (original) A router as claimed in claim 1 where the second set of buffers holds information units for a complete set of virtual channels.

4. (previously presented) A router as claimed in claim 1 wherein the first set of buffers comprises:

a buffer pool shared by channels; and

a pointer array of pointers, associated with individual channels, to buffered information units.

5. (original) A router as claimed in claim 1 wherein the first set of buffers is organized as a set-associative cache.

6. (original) A router as claimed in claim 5 wherein each entry in the set associative cache contains a single information unit.

7. (original) A router as claimed in claim 5 wherein each entry in the set associative cache contains the buffers and state for an entire virtual channel.

8. (original) A router as claimed in claim 1 further comprising flow control to stop the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers.

9. (original) A router as claimed in claim 8 wherein the flow control is blocking.

10. (original) A router as claimed in claim 8 wherein the flow control is credit-based.

11. (previously presented) A router including buffers, for information units transferred through the router, comprising:

a first set of rapidly accessible buffers which store information units received at an input link;

a second set of buffers for the information units that are accessed more slowly than the first set; and

miss status registers to hold information units waiting for access to the second set of buffers.

12. (previously presented) A router including buffers, for information units transferred through the router, comprising:

a first set of rapidly accessible buffers which store information units received at an input link;

a second set of buffers for the information units that are accessed more slowly than the first set; and

an eviction buffer to hold entries staged for transfer from the first set of buffers to the second set of buffers.

13. (original) A router as claimed in claim 1 in a multicomputer interconnection network.

14. (previously presented) A router as claimed in claim 1 wherein the router is a fabric router.

15. (original) A router as claimed in claim 1 wherein the router is a fabric router and the information units are flits.

16. (previously presented) A method of buffering information units in a router comprising:

storing the information units received at an input link in a first set of rapidly accessible buffers; and

storing overflow from the first set of buffers in a second set of buffers that are accessed more slowly than the first set;

the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.

17. (original) A method as claimed in claim 16 wherein

the router is implemented on one or more integrated circuit chips;

the first set of buffers are located on the router integrated circuit chips; and

the second set of buffers are located on memory chips separate from the router integrated circuit chips.

18. (original) A method as claimed in claim 16 where the second set of buffers holds information units for a complete set of virtual channels.

19. (original) A method as claimed in claim 16 further comprising, in the first set of buffers, storing the information units in a buffer pool shared by channels and pointing to information units within the buffer pool from an array of pointers associated with individual channels.

20. (original) A method as claimed in claim 16 wherein the first set of buffers is organized as a set-associative cache.

21. (original) A method as claimed in claim 20 wherein each entry in the set associative cache contains a single information unit.

22. (original) A method as claimed in claim 20 wherein each entry in the set associative cache contains the information unit buffers and state for an entire virtual channel.

23. (original) A method as claimed in claim 16 further comprising controlling flow to stop the arrival of new information units while transferring flits between the first set of buffers and the second set of buffers.

24. (original) A method as claimed in claim 23 wherein the flow control is blocking.

25. (original) A method as claimed in claim 23 wherein the flow control is credit-based.

26. (previously presented) A method of buffering information units in a router comprising:

storing the information units received at an input link in a first set of rapidly accessible buffers;

storing overflow from the first set of buffers in a second set of buffers that are accessed more slowly than the first set; and

storing information units waiting for access to the second set of buffers in miss status registers.

27. (previously presented) A method of buffering information units in a router comprising:

storing the information units received at an input link in a first set of rapidly accessible buffers;

storing overflow from the first set of buffers in a second set of buffers that are accessed more slowly than the first set; and

storing information units staged for transfer from the first set of buffers to the second set of buffers in an eviction buffer.

28. (original) A method as claimed in claim 16 wherein the router is in a multicomputer interconnection network.

29. (canceled)

30. (original) A method as claimed in claim 16 wherein the router is a fabric router and the information units are flits.

31. (previously presented) A network comprising a plurality of interconnected routers, each router including information unit buffers comprising:

a first set of rapidly accessible information unit buffers which store information units received at an input link; and

a second set of information unit buffers which store the information units and that are accessed more slowly than the first set;

the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.

32. (original) A network as claimed in claim 31 wherein:

the router is implemented on one or more integrated circuit chips;

the first set of buffers are located on the router integrated circuit chips; and

the second set of buffers are located on memory chips separate from the router integrated circuit chips.

33. (original) A network as claimed in claim 31 where the second set of buffers holds information units for a complete set of virtual channels.

34. (previously presented) A network as claimed in claim 31 wherein the first set of buffers comprises:

a buffer pool shared by channels; and

a pointer array of pointers, associated with individual channels, to buffered information units.

35. (original) A network as claimed in claim 31 wherein the first set of buffers is organized as a set-associative cache.

36. (original) A network as claimed in claim 31 further comprising flow control to stop the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers.

37. (original) A network as claimed in claim 31 further comprising flow control to stop the arrival of new information units while transferring flits between the first set of buffers and the second set of buffers.

38. (previously presented) A network as claimed in claim 31 wherein the router is a fabric router.

39. (original) A network as claimed in claim 31 wherein the router is a fabric router and the information units are flits.

40. (previously presented) A router comprising:

means for storing information units received at an input link in a first set of rapidly accessible buffers; and

means for storing information units in a second set of buffers that are accessed more slowly than the first set;

the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.

41. (original) A router as claimed in claim 40 where the second set of buffers holds information units for a complete set of virtual channels.

42. (original) A router as claimed in claim 40 wherein the first set of buffers comprises:

a buffer pool shared by channels; and

means for pointing to entries in the buffer pool for individual channels.

43. (original) A router as claimed in claim 40 wherein the first set of buffers is organized as a set-associative cache.

44. (original) A router as claimed in claim 40 further comprising means for providing flow control for stopping the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers.

45. (original) A router as claimed in claim 40 wherein the router is a fabric router and the information units are flits.

46. (previously presented) A router as claimed in claim 40 wherein the buffers of the first set of rapidly accessible buffers are dynamically assignable to virtual channels to serve as a virtual channel buffer cache.

47. (previously presented) A router as claimed in claim 1 wherein the buffers of the first set of rapidly accessible buffers are dynamically assignable to virtual channels to serve as a virtual channel buffer cache.

48. (previously presented) A method as claimed in claim 16 wherein the buffers of the first set of rapidly accessible buffers are dynamically assignable to virtual channels to serve as a virtual channel buffer cache.

49. (previously presented) A network as claimed in claim 31 wherein the buffers of the first set of rapidly accessible buffers are dynamically assignable to virtual channels to serve as a virtual channel buffer cache.

50. (previously presented) A router as claimed in claim 40 further comprising means to arbitrate for plural information units to access an output channel.

51. (previously presented) A router as claimed in claim 1 wherein an arbitration provides access of plural information units to an output channel.

52. (previously presented) A method as claimed in claim 16 wherein an arbitration provides access of plural information units to an output channel.

53. (previously presented) A network as claimed in claim 31 wherein an arbitration provides access of plural information units to an output channel.

54. (new) A router as claimed in claim 1 comprising a separate buffer array of first and second sets of buffers for each input port.

55. (new) A method as claimed in claim 16 wherein a separate buffer array of first and second sets of buffers is provided for each input port.

56. (new) A method as claimed in claim 31 comprising a separate buffer array of first and second sets of buffers for each input port.